Towards Electronic-Photonic Design Automation for Optical Interconnect Networks

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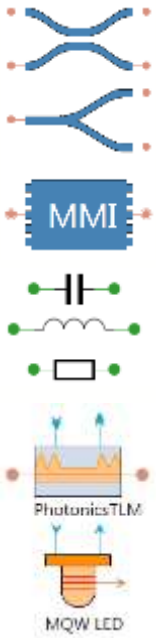
Outline

- Motivation
  - Need of flexible electronic-photonics automation tools (EPDA)
  - Already existing electronic (EDA) and photonic (PDA) tools
    - Mature
    - Built upon established approaches & user expectations
- Layout-aware schematic-driven design
- Layout-aware macro scripting
- EDA-PDA integration
  - Mentor Graphics (Pyxis Schematic) ⇆ VPI Design Suite
  - Cross-platform cosimulation example
  - Workflow integration

Photonic Circuit Design & Analysis
Automated Design Environment



Graphical User Interface

Circuit Topology Graphical Editor | Parameter Editor | Topology Scripting

Remote Servers, Resources Management

Compound Hierarchical Models

Behavioral & Analytical | Measured | Custom Programmed

Advanced Parameter Scripting

Simulation Domains

Opto-electronics | Dynamic Tunable Photonics | Passive Photonics | Linear Electronics

Hybrid-Domain | Time-Domain | Frequency-Domain

TLM, IIR/FIR, S-Matrix assembly, Multi-core CPU parallelization

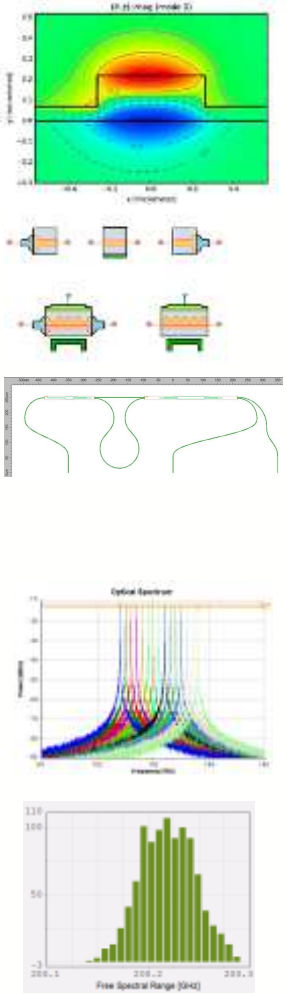
Simulation Control, Optimization & Analysis

Advanced Visualization | Instrumentation & Analysis Tools | Parameter Sweeps | Simulation Scripting | Simulation Engine Driver

Sensitivity and Yield Analysis

VPIphotonics & partners

- Device-level Simulators
- Process Design Kits
- Layout & Mask Design
- Nonlinear Electronics
- EDA Cosimulation

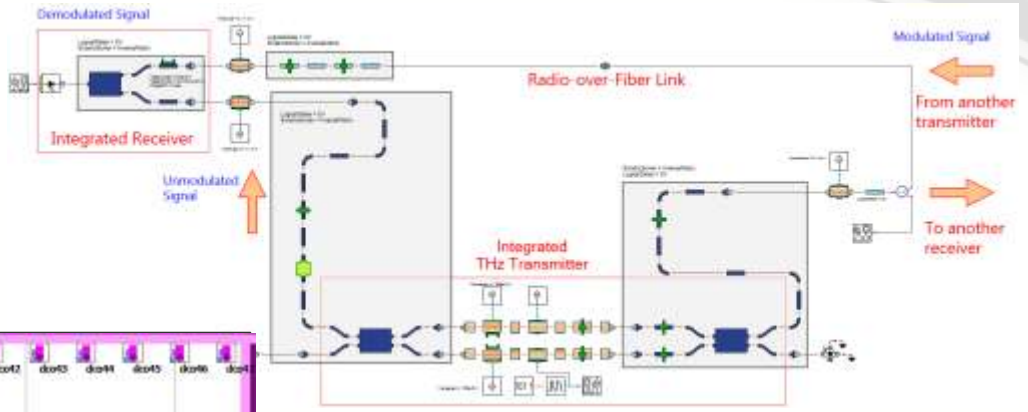


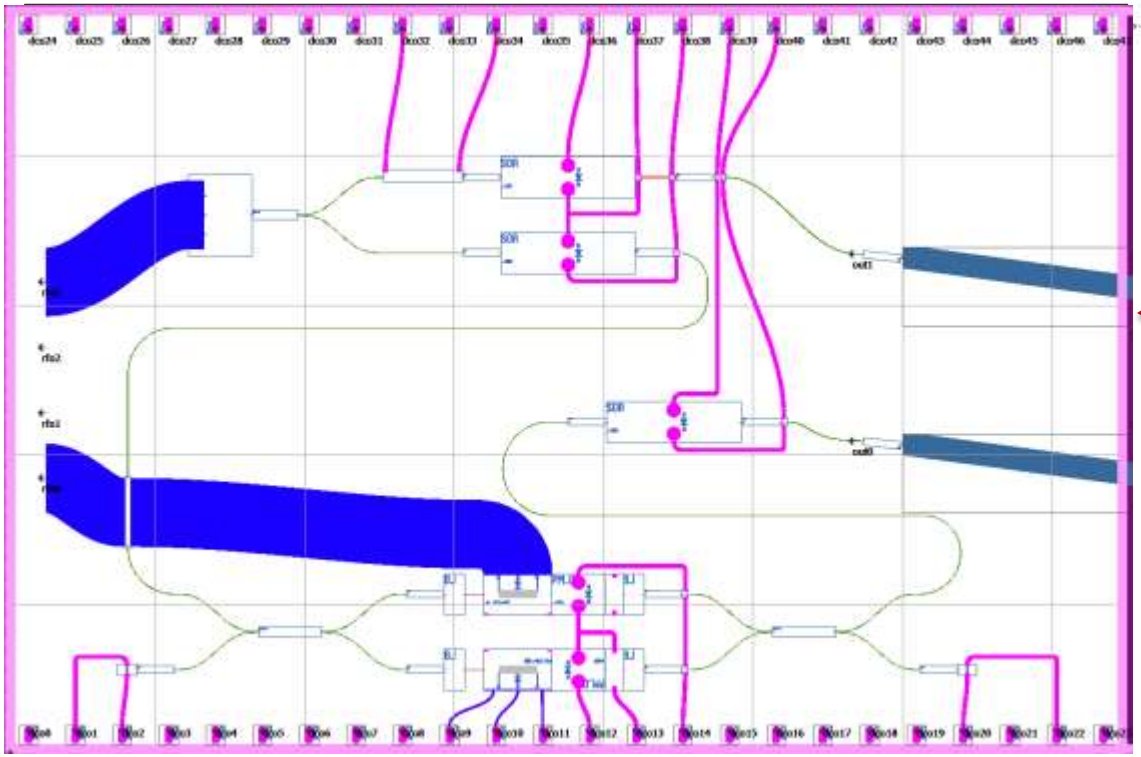
Circuit or Layout first?

Circuit Simulation	Layout Design
What to start with?	
Schematic-driven design methodology?	*Layout-driven design methodology?*
Design Characteristics	Final Layout

Schematic-driven Design Example: Integrated THz Transceiver

Automated export of intermediate or final circuit designs to PhoeniX' OptoDesigner for layout design and GDSII-file generation





- ✓ Export of final circuit design
- ✓ Adding packaging and GDSII mask generation

Based on idea from:
F.M. Soares et al., *Transmitter PIC for THz Applications Based on Generic Integration Technology*, IPRM2013, Kobe, Japan.

Schematic-driven design: why not sufficient?

Standard schematic-driven approach

- BB layout determined by its parameters (length, bend angle, etc.)

⇨ IC layout fully determined by connectivity between BBs

⇨ Allows immediate IC simulation as BB model is known at each design step

BB – Building Block
IC - Integrated Circuit

Two roles of optical waveguides

- Could act as connecting device: routes optical signals between building blocks of the circuit

⇨ Detailed properties (length, width, shape) are not critical, may be ignored

- Could act as functional device: determine interference between signals traveling in different paths

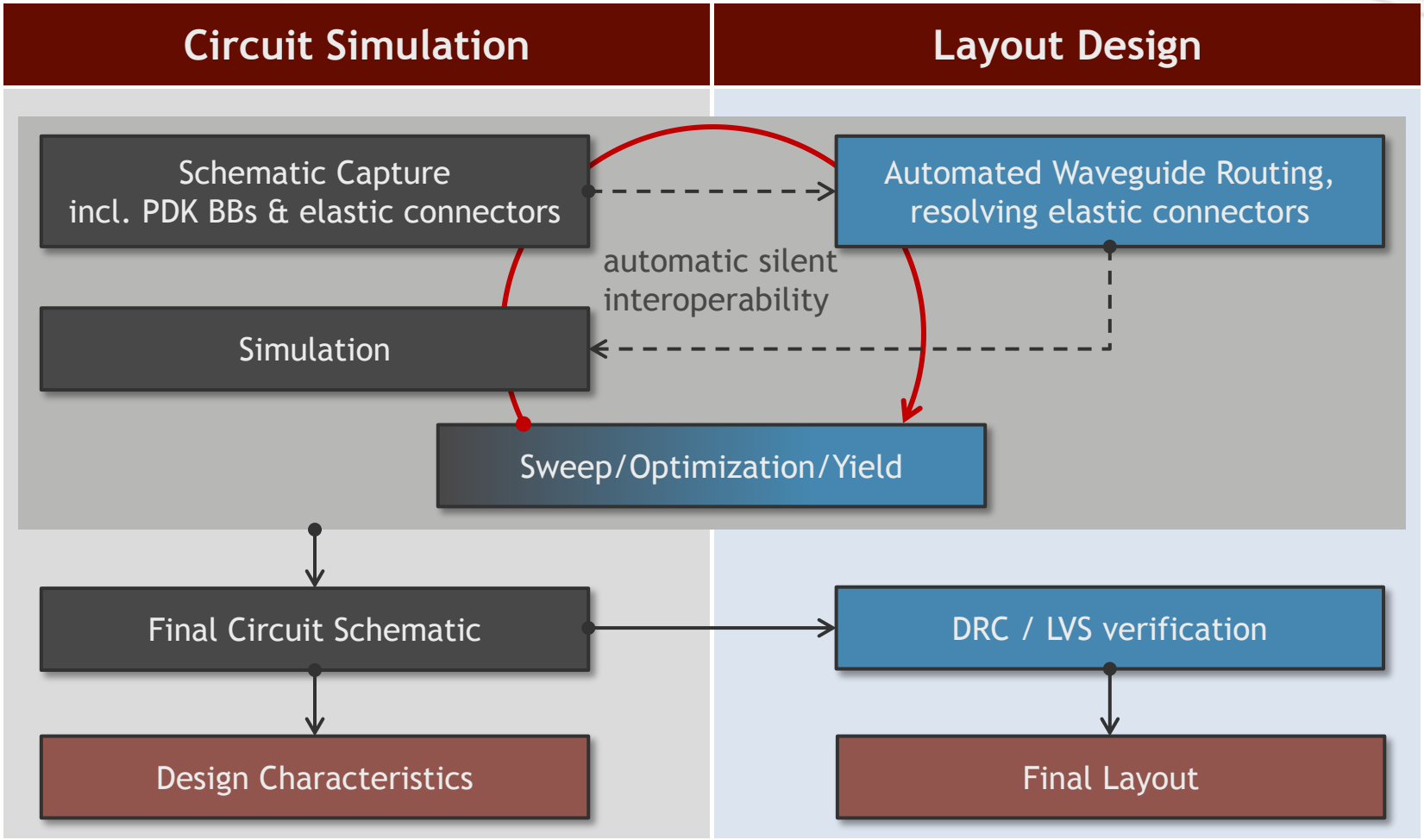
⇨ Detailed properties are very important, already at the beginning of circuit design

Problem: Often, no clear separation possible!

Photonic IC design ≠ circuit design + layout design

⇨Tight interaction between layout and circuit design necessary

Interoperation of Circuit & Layout

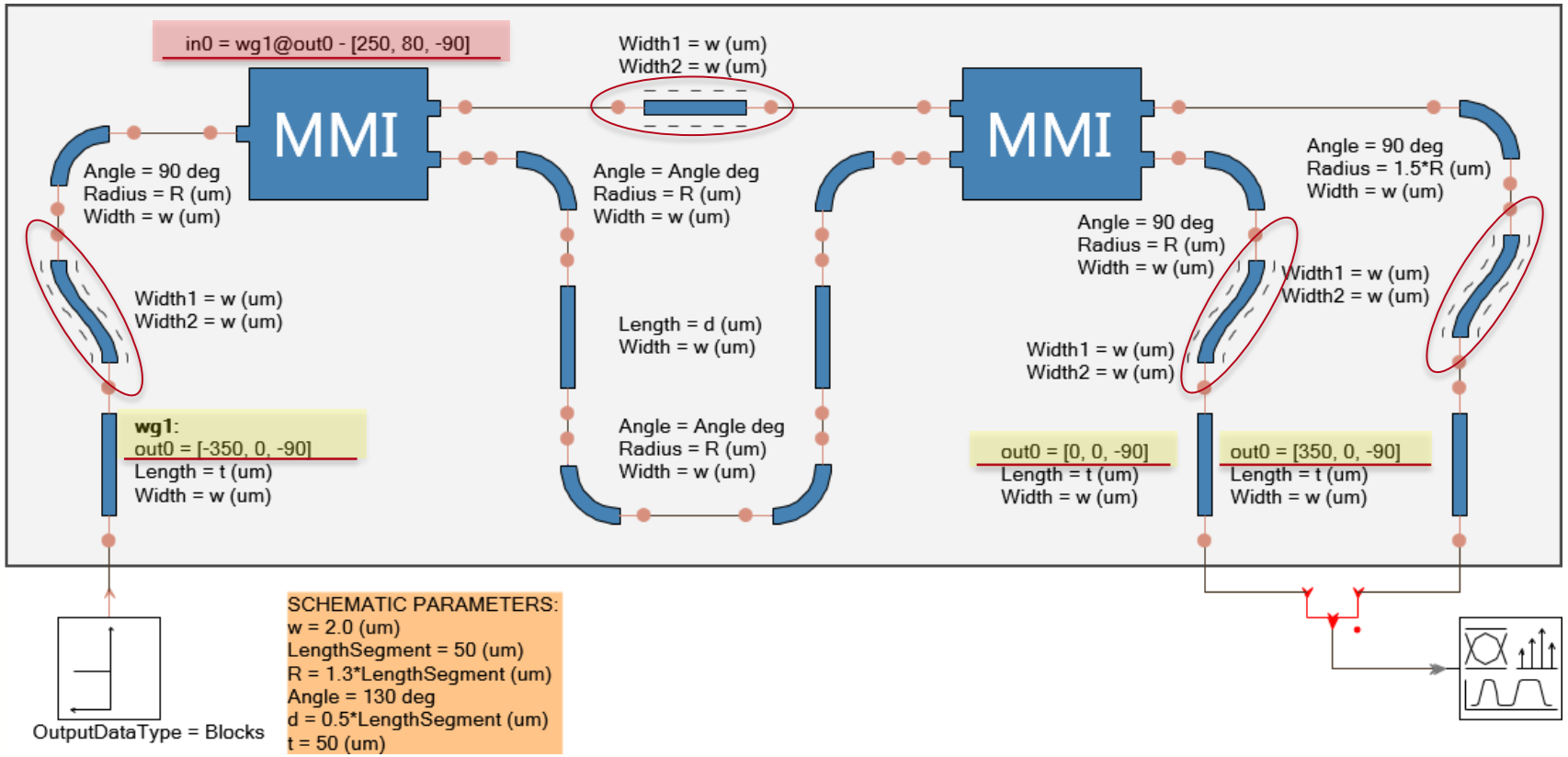


Layout-aware schematic-driven design methodology enables transparent access to information and functions

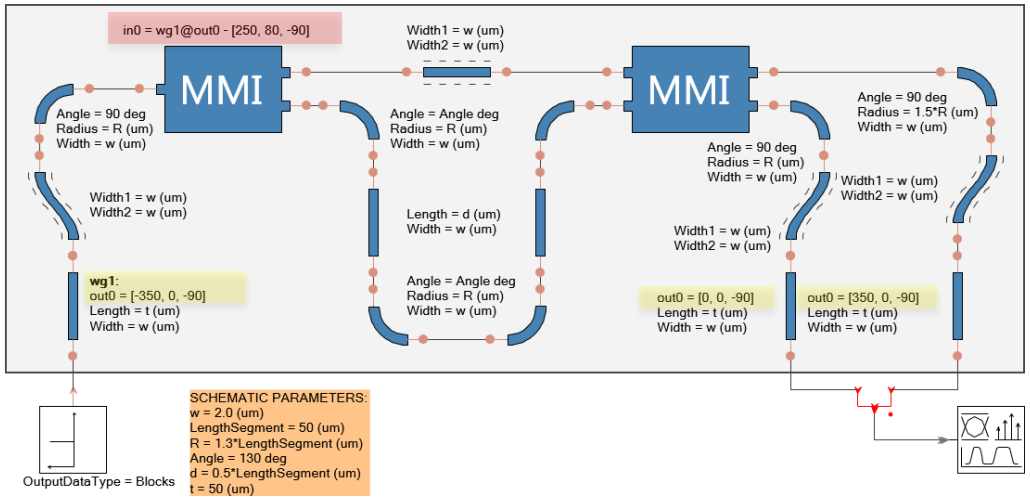
Layout-aware Circuit Design

Circuit design of unbalanced Mach-Zehnder interferometer

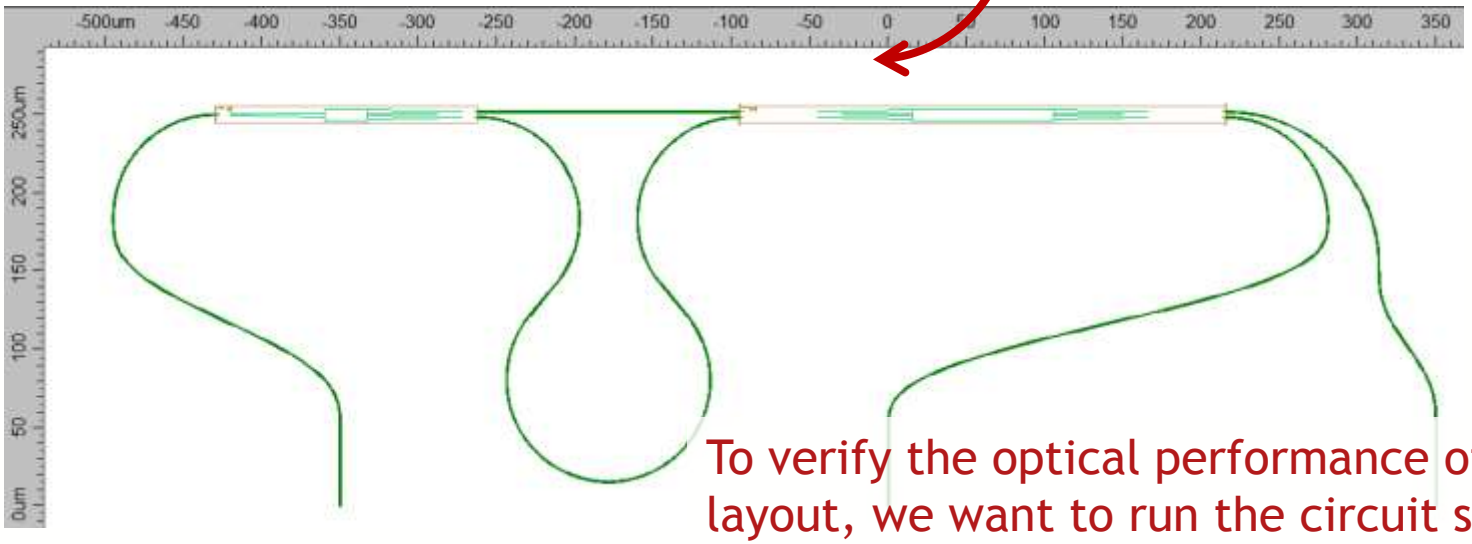
- use elastic connectors (dimensions defined by layout)
- specify desired locations for some of the ports



Automated Export to Layout Design Tool

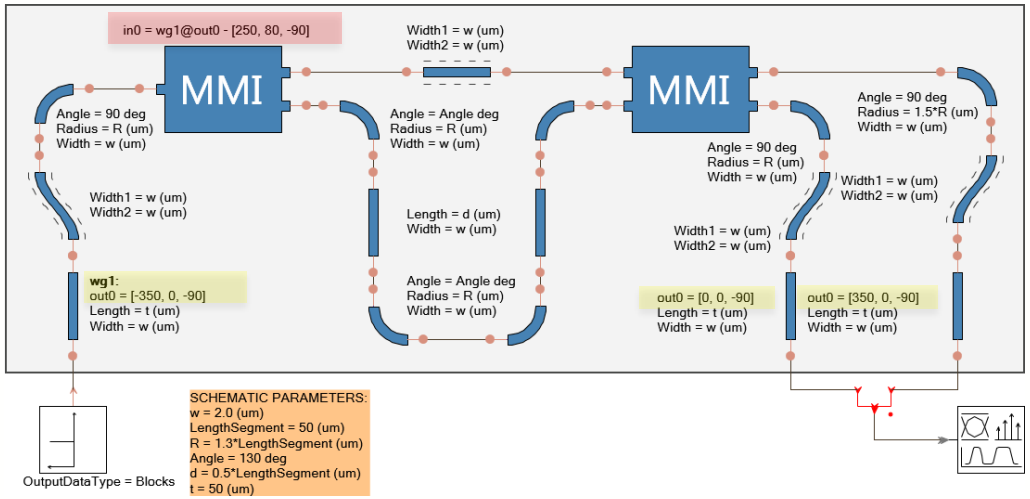


Automated export of layout with elastic connectors (*Export to OptoDesigner* macro)

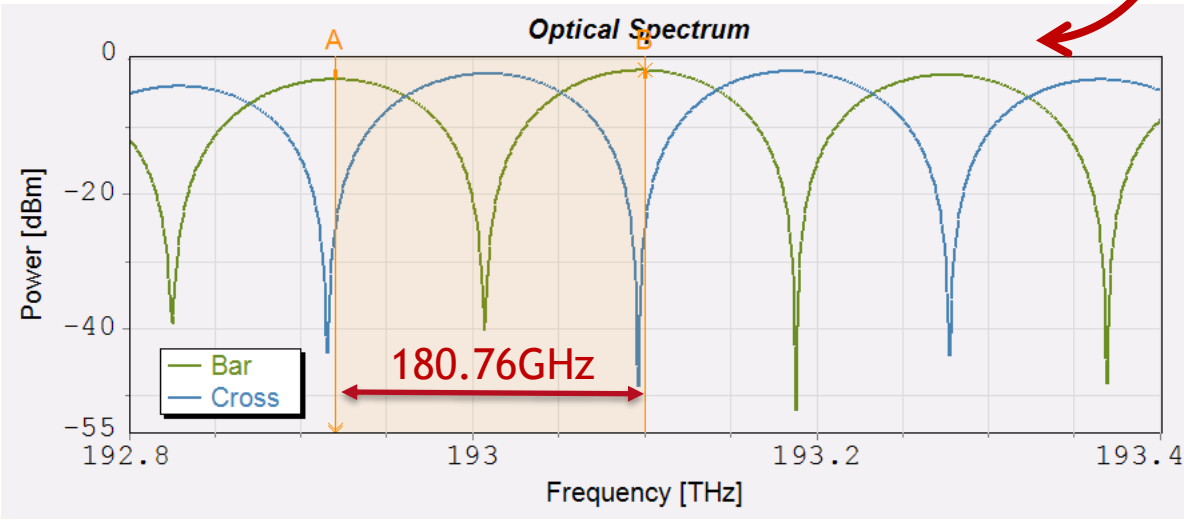


To verify the optical performance of the layout, we want to run the circuit simulation.

Simulation of Circuits with Elastic Connectors



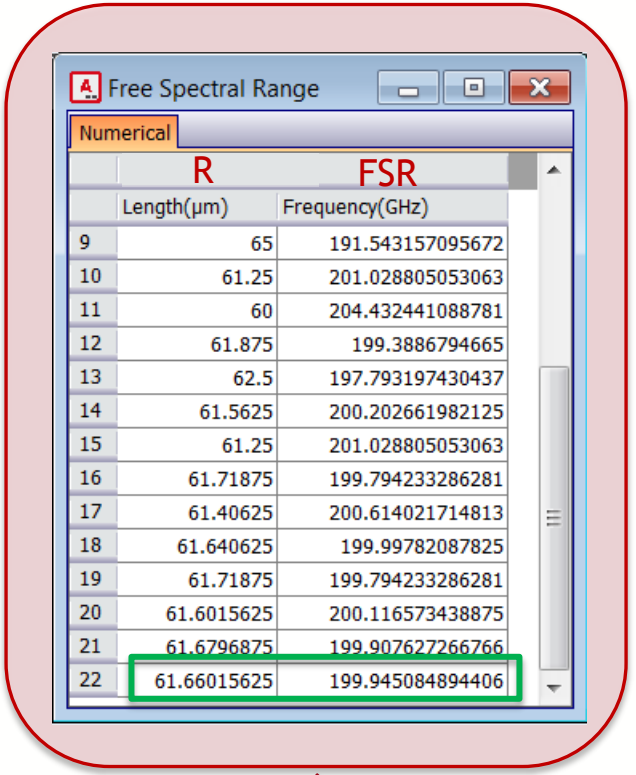
Circuit simulations with elastic connectors (*Run Resolving Elastic* macro)

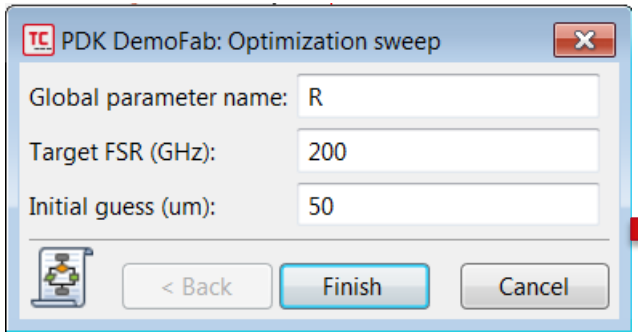


Values of elastic connectors calculated in *OptoDesigner* (available in message log after simulation)

Layout-aware schematic driven approach: further actions

- Layout optimization & sweep
  - Example: automatic optimization of FSR
- Yield analysis
- Interaction with layout tool
  - Automatic
  - Before every photonic simulation
  - Guarantee correctness





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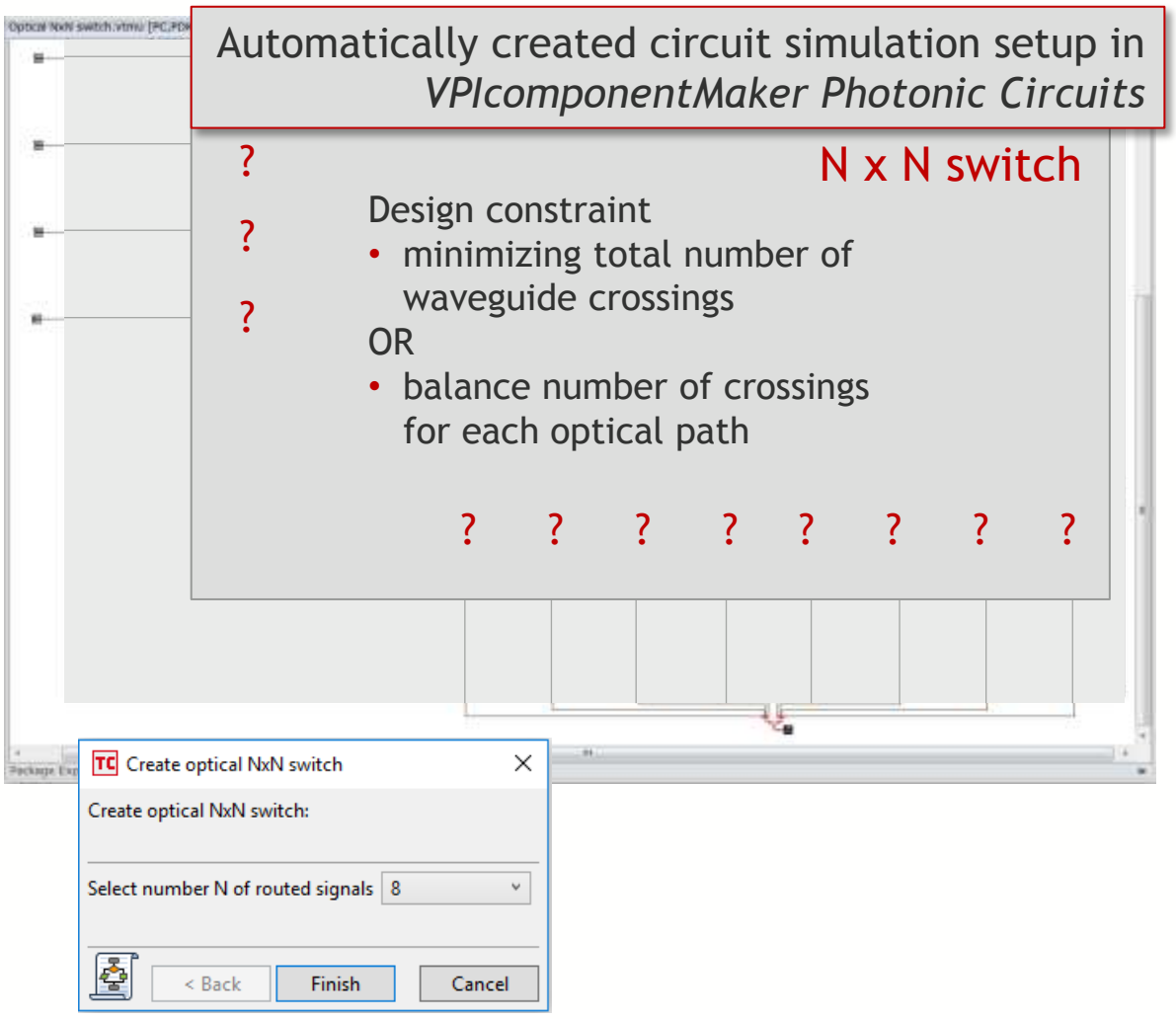
Large-scale integration: Layout-Aware Macro Scripting



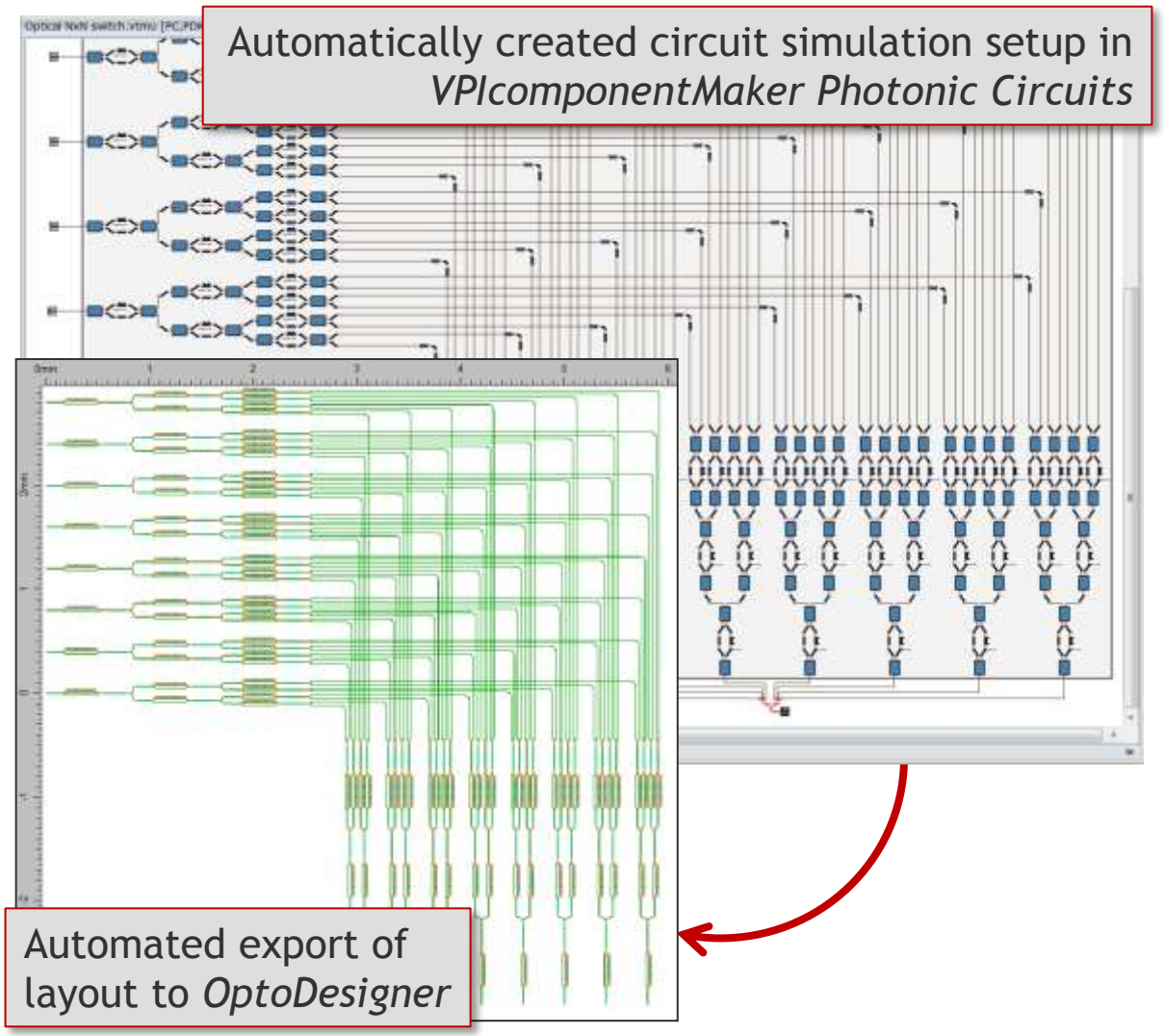
Optical interconnect switching networks

Design of very large-scale photonic ICs becomes very inefficient by manually placing building blocks and interconnecting them.

Utilize macro scripting with set of “layout-aware” commands, which allow to determine physical locations and orientations of building block ports on layout, etc.

With this, circuit design is created automatically

Large-scale integration: Layout-Aware Macro Scripting



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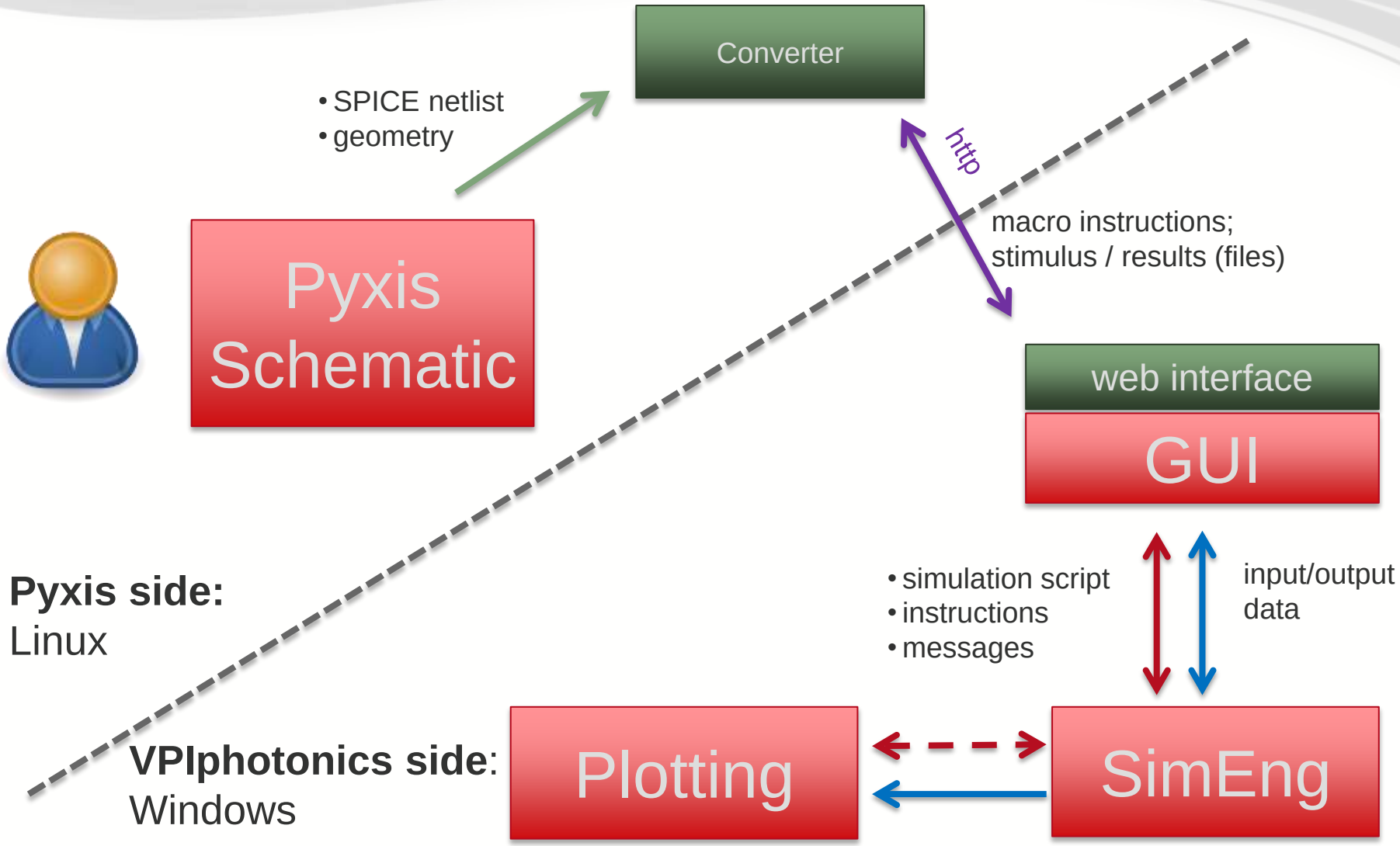
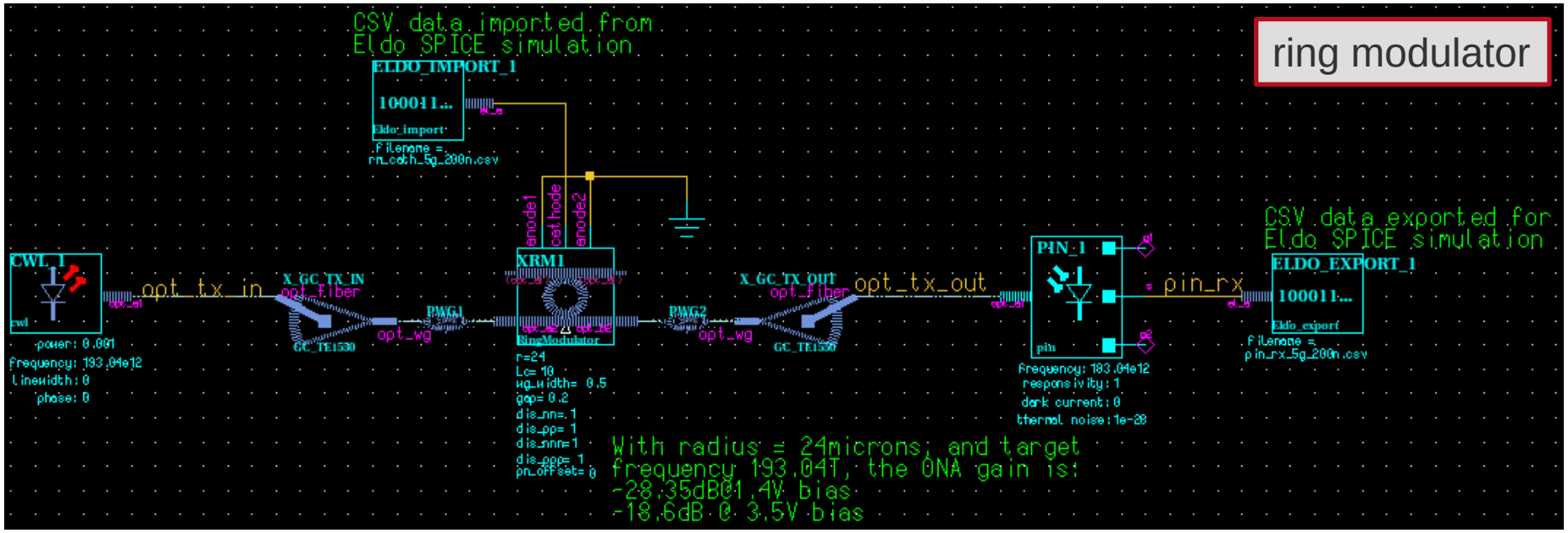
Integration Example



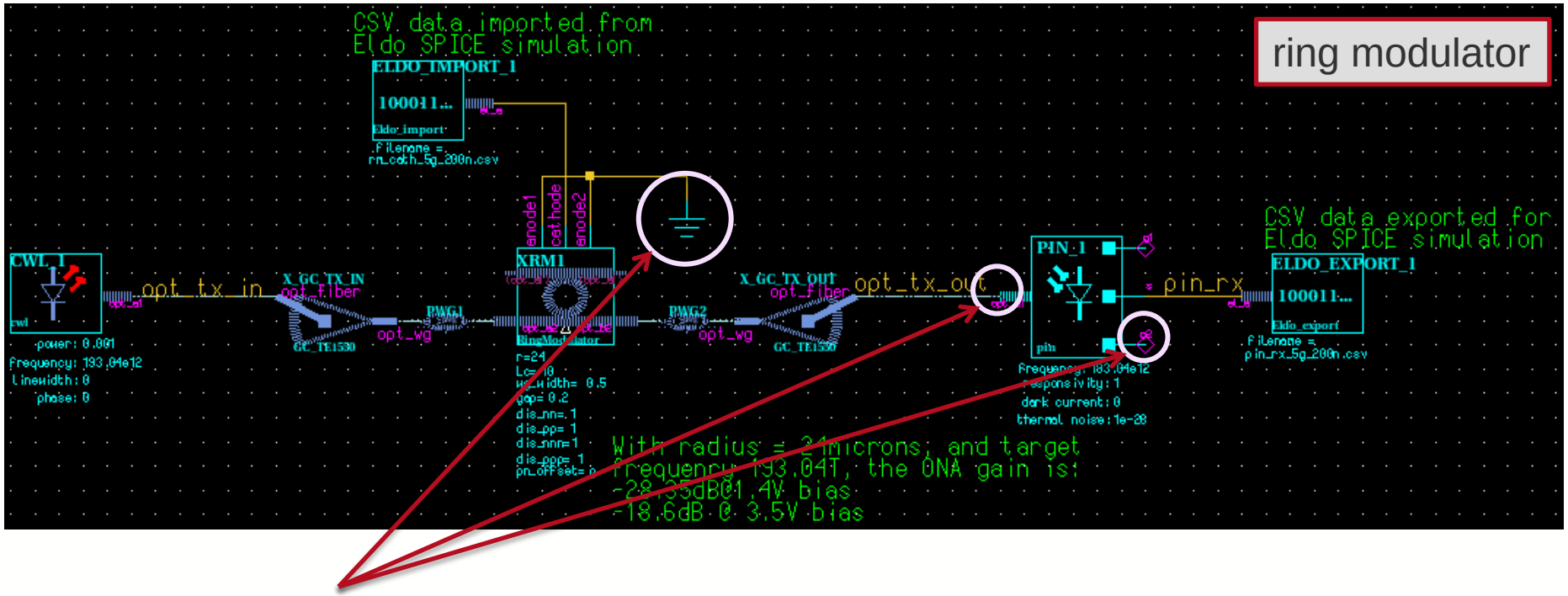
Use-case

Schematic on Pyxis side:



Issues

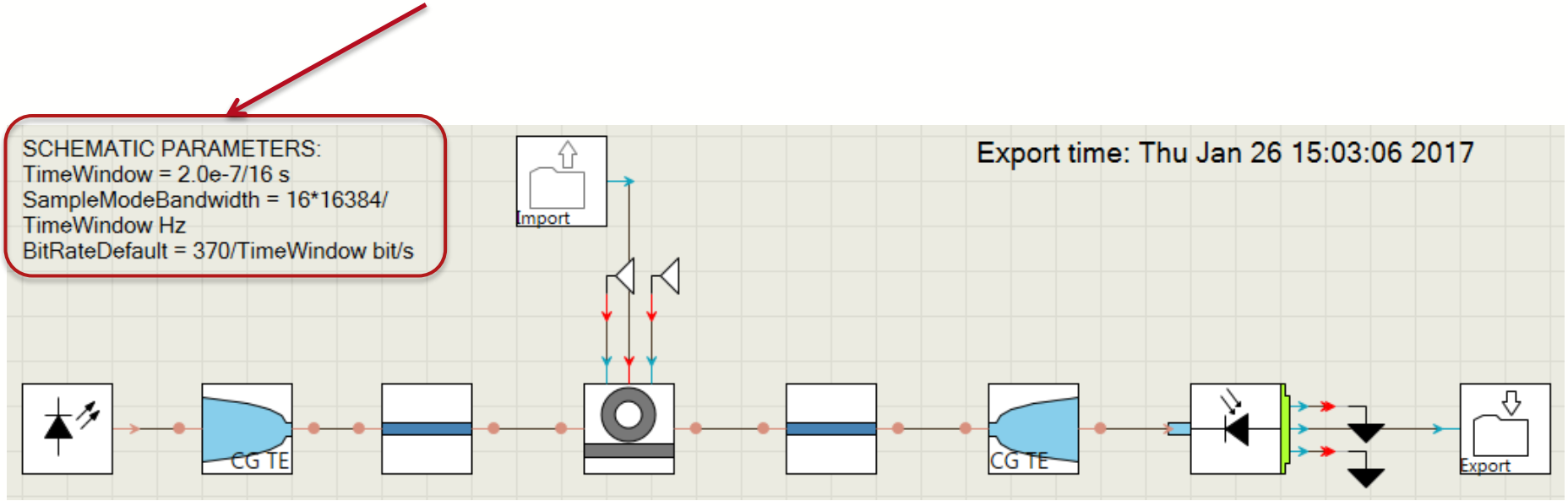
Schematic on Pyxis side:



(Electrical) ground (set globally)
Bidirectional ports
Non-connected pins

Conversion result

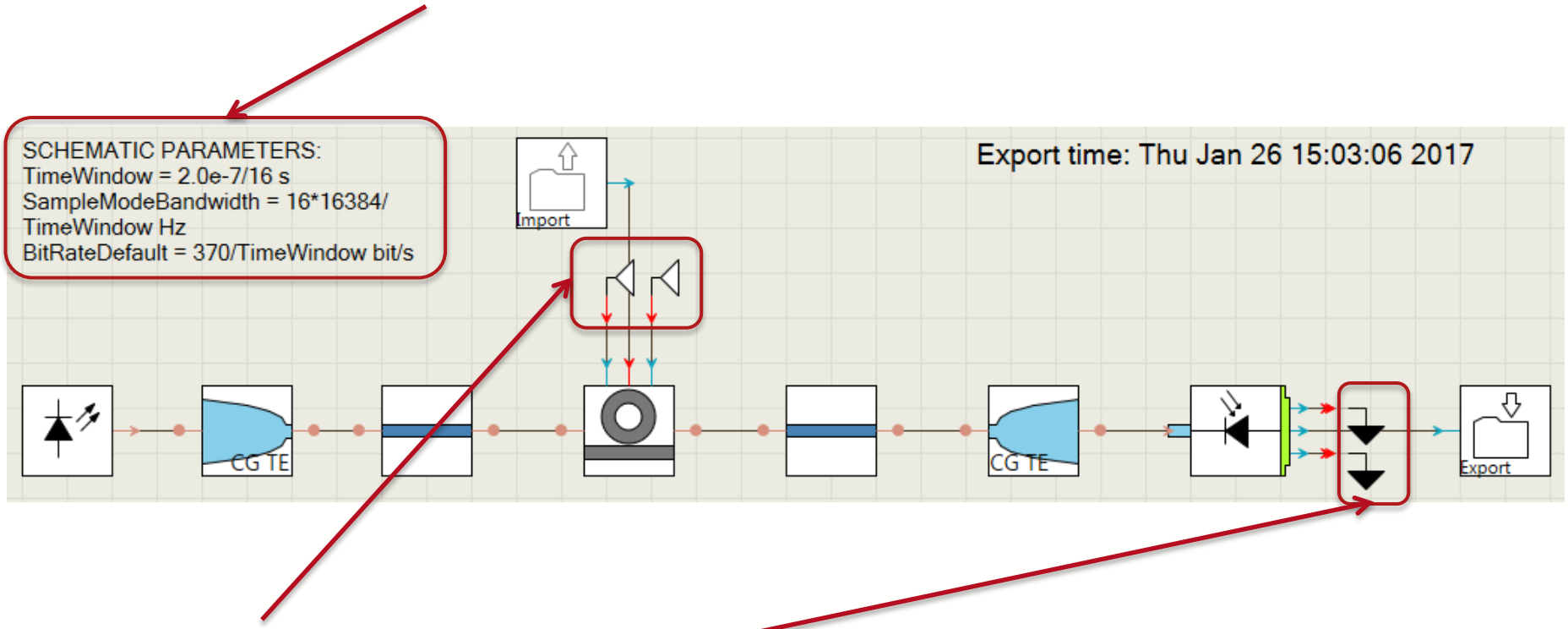
Simulation duration specified separately



- External specification of simulation duration
  - **TimeWindow** parameter
- Exchange of files
  - E-O-E simulation
  - File transfer over network
  - Reading of the whole stimulus file

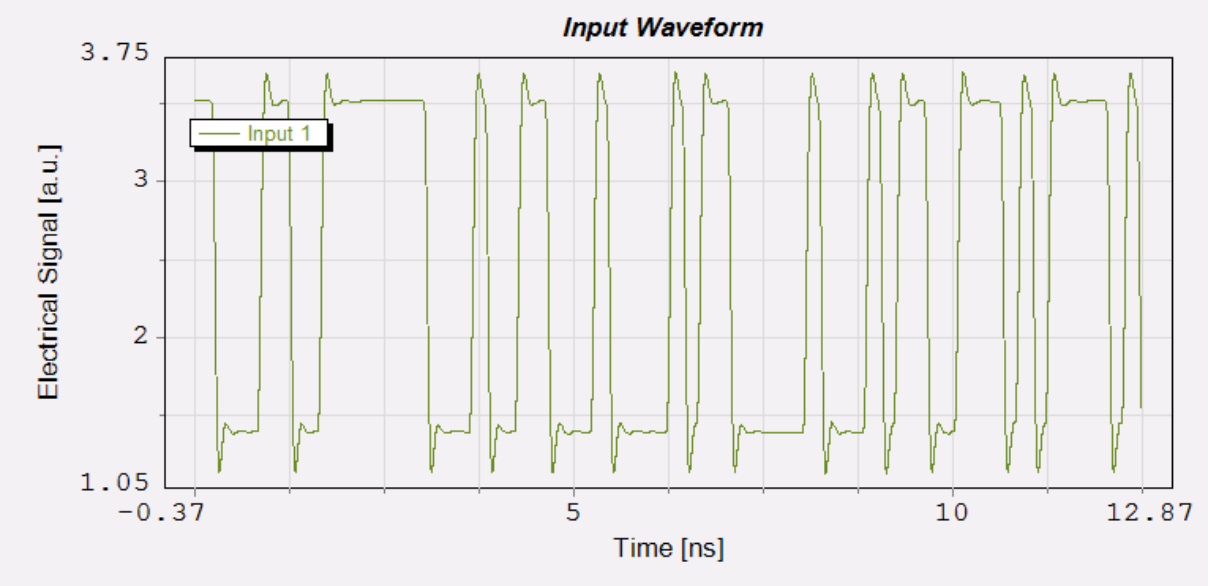
Conversion result

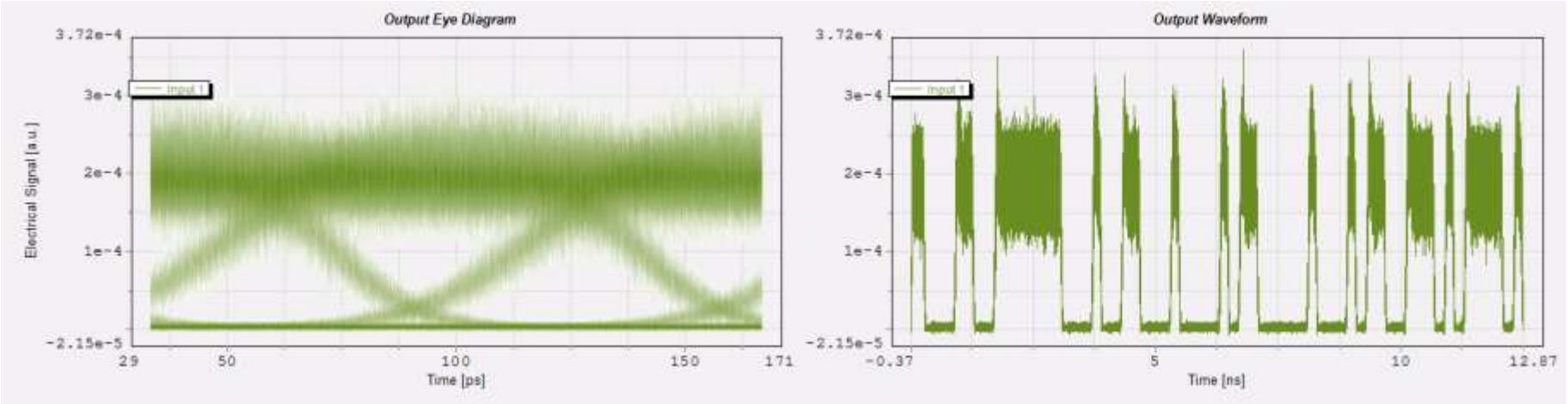
Simulation duration specified separately



Unused pins terminated by converter

Simulation result

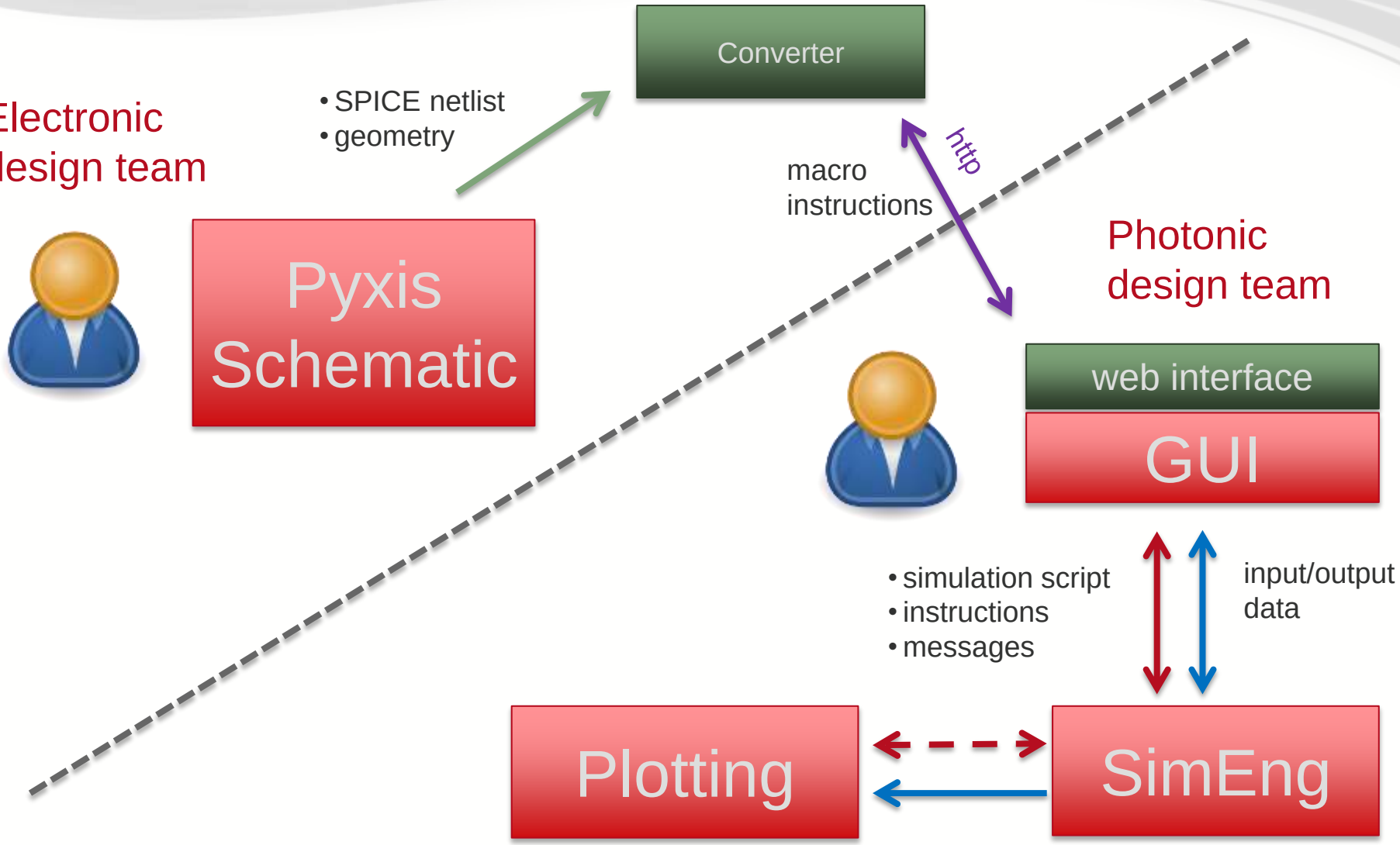




Cross-team design automation

- Photonic vs. electronic design frequently requires
  - Different skills
  - Different PDKs
  - Specific analysis approaches
- Cross-team: design is used by another team for analysis

Integration Approach



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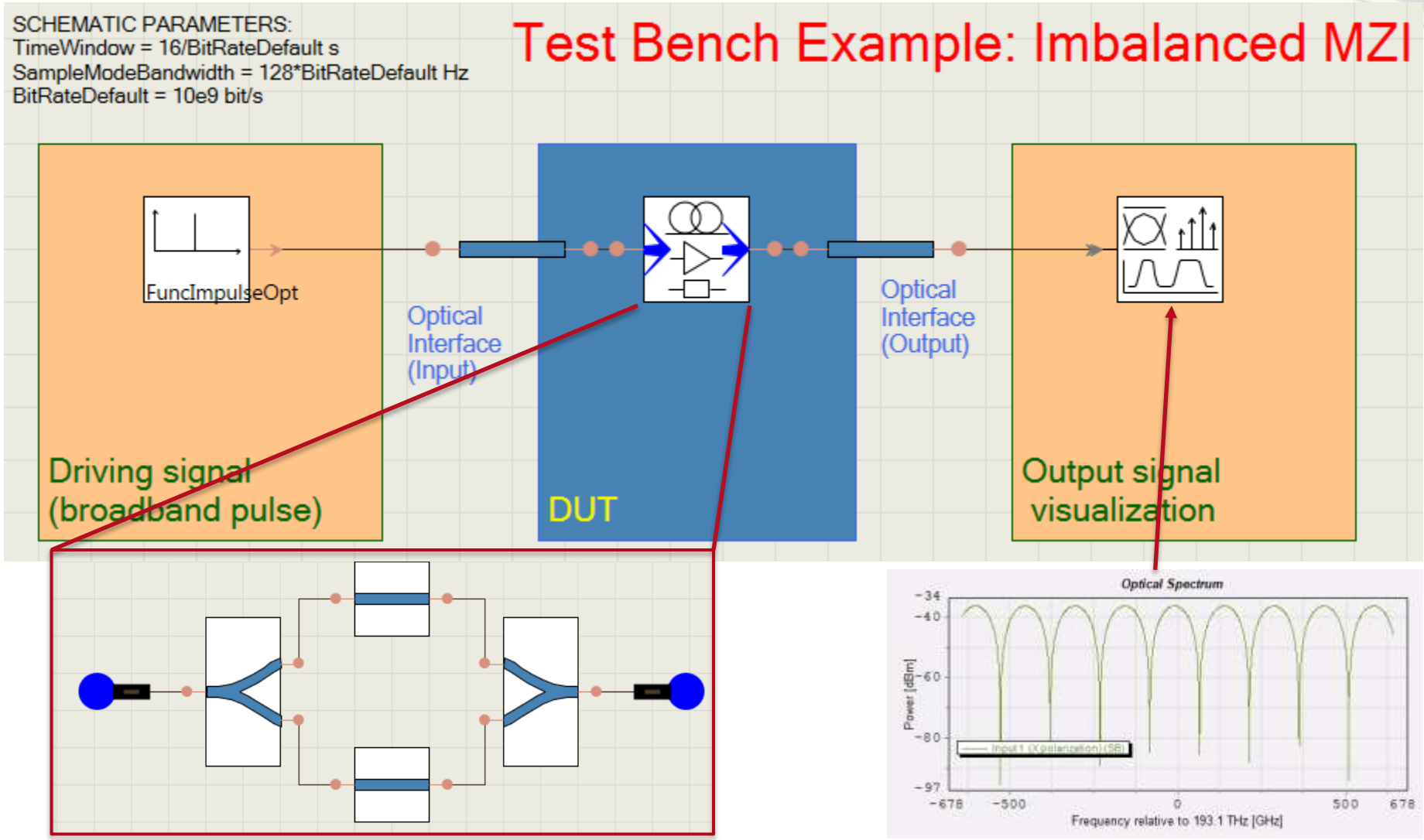

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Summary

- *Progress in optical interconnection* requires changes in design approach
  - EDA and PDA are already mature tools built upon different approaches
  - seamless integration requires clearly defined interfaces
  - support of cross-platform and cross-team work
- *Layout-aware schematic-driven design* methodology
  - seamless integration of circuit and layout design tools
  - flexible and adaptive definition of PDK libraries
- *Next steps* towards
  - full interoperation / integration of electronic, photonic and layout design tools

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